

N-Channel JFET Monolithic Dual



U440 / U441

FEATURES

- High Gain $g_{fs} > 6 \text{ mS}$
- Low Leakage $I_g < 1 \text{ pA typical}$
- Low Noise

APPLICATIONS

- Differential Wideband Amplifiers
- VHF/UHF Amplifiers
- Test and Measurement
- Multi-Chip/Hybrids

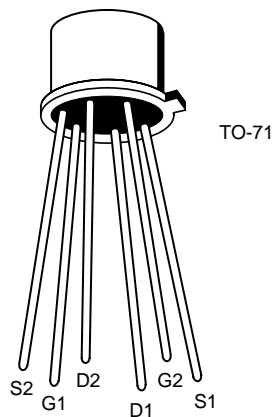
DESCRIPTION

The U440 Series is an N-Channel Monolithic Dual JFET designed for high speed amplifier circuits. Featuring high gain ($> 6 \text{ mS typical}$), low leakage ($< 1 \text{ pA typ}$) and low noise. This series is an excellent choice for differential amplifier designs.

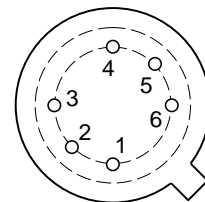
ORDERING INFORMATION

Part	Package	Temperature Range
U440-1	Hermetic TO-71 Package	-55°C to +150°C
XU440-1	Sorted Chips in Carriers	-55°C to +150°C

PIN CONFIGURATION



- 1 SOURCE 1
- 2 DRAIN 1
- 3 GATE 1
- 4 SOURCE 2
- 5 DRAIN 2
- 6 GATE 2



BOTTOM VIEW

CJ1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	V
Gate-Gate Voltage	V_{GG}	± 50	V
Forward Gate Current	I_G	50	mA
Power Dissipation (per side)	P_D	250	mW
(total)		350	mW
Power Derating (per side)		2	mW/°C
(total)		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 200	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP ¹	U440		U441		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
STATIC								
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	-35	-25		-25		V	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$
$V_{GS(OFF)}$	Gate-Source Cut off Voltage	-3.5	-1	-6	-1	-6		$V_{DS} = 10\text{V}, I_D = 1\text{nA}$
I_{DSS}	Saturation Drain Current ²	15	6	30	6	30	mA	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate Reverse Current	-1		-500		-500	pA	$V_{GS} = -15\text{V}, V_{DS} = 0\text{V}$
		-2					nA	$T_A = 150^\circ\text{C}$
I_G	Gate Operating Current	-1		-500		-500	pA	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
		-0.3					nA	$T_A = 125^\circ\text{C}$
$V_{GS(F)}$	Gate-Source Forward Voltage	0.7					V	$I_G = 1\text{mA}, V_{DS} = 0\text{V}$
DYNAMIC								
g_{fs}	Common-Source Forward Transconductance	6	4.5	9	4.5	9	mS	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{kHz}$
g_{os}	Common-Source Output Conductance	70		200		200	μS	
C_{iss}	Common-Source Input Capacitance	3					pF	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance	1						
\bar{e}_n	Equivalent Input Noise Voltage	4					nV/√Hz	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 10\text{kHz}$
MATCHING								
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	6		10		20	mV	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Change with Temperature	20					$\mu\text{V}/^\circ\text{C}$	$T = -55$ to 25°C
		20						$T = 25$ to 125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.97						$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97						$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{kHz}$
CMRR	Common Mode Rejection Ratio	85					dB	$V_{DD} = 5$ to $10\text{V}, I_D = 5\text{mA}$

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; $PW = 300\mu\text{s}$, duty cycle $\leq 3\%$.